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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,016	10/28/2003	Vikram Joshi	13176.403D1US (.459)	4266
24283	7590	08/13/2004	EXAMINER	
PATTON BOGGS 1660 LINCOLN ST SUITE 2050 DENVER, CO 80264			WILLE, DOUGLAS A	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 08/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/695,016

**Applicant(s)**

JOSHI ET AL.

**Examiner**

Douglas A Wille

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 28 October 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 43-59 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 43-59 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>0204</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claim 43 is rejected under 35 U.S.C. 102(a) as being anticipated by Bailey.

3. With respect to claim 43, Bailey shows a method of fabricating an IC (see cover Figure and column 6, line 41 et seq.) with a substrate (not numbered), a switch transistor, a first insulating layer of BPSG (column 6, line 60), a nonconducting buried diffusion barrier of  $\text{Si}_3\text{N}_4$  (column 13, line 31) and a second insulating layer 1176 of UTEOS.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 44 – 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bailey in view of Asano et al.

6. With respect to claim 44, Bailey shows a conductive plug contacting the switch with CMP being performed after the plug formation (see Figure 10A). Bailey does not specify that CMP is performed after other steps in the process but the use of CMP would be obvious in any case where the processed surface were insufficiently flat and would be performed for the same

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reason that the CMP shown is used. Bailey shows the use of a hydrogen barrier and Asano et al. show that oxygen can have deleterious effects and provides an oxygen barrier below the capacitor lower electrode (see cover Figure and column 17, line 30). It would be obvious to include an oxygen barrier in the Bailey device to prevent deleterious effects of oxygen as shown by Asano et al. Bailey shows a bottom electrode 1178, a dielectric 1180 and a top electrode 1182. Although it is not clearly shown by Bailey, the resultant structure would obviously require etching the capacitor stack.

7. With respect to claim 45, Bailey shows a third insulating layer surrounding the capacitor, the third layer having an opening for a plate line electrode 192 and portions of the layers are removed to provide for the electrode contact shown to the right of the capacitor.

8. With respect to claim 46, the hydrogen barrier surrounds the capacitor.

9. With respect to claim 47, the hydrogen barrier is only on the capacitor and would obviously have been removed from the rest of the device.

10. With respect to claim 48, there is a connection to the plate line and there is a connection to the switch.

11. With respect to claim 49, Bailey shows the use of a hydrogen barrier and Asano et al. show that oxygen can have deleterious effects and provides an oxygen barrier below the capacitor lower electrode (see cover Figure and column 17, line 30). It would be obvious to include an oxygen barrier in the Bailey device to prevent deleterious effects of oxygen as shown by Asano et al. Bailey shows a bottom electrode 1178, a dielectric 1180 and a top electrode 1182. There is a plate line electrode (cover Figure) and the hydrogen barrier is on the electrode and surrounds the capacitor.

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12. With respect to claim 50, Bailey shows a conductive plug contacting the switch with CMP being performed after the plug formation (see Figure 10A). Bailey does not specify that CMP is performed after other steps in the process but the use of CMP would be obvious in any case where the processed surface were insufficiently flat and would be performed for the same reason that the CMP shown is used. Bailey shows a bottom electrode 1178, a dielectric 1180 and a top electrode 1182. Although it is not clearly shown by Bailey, the resultant structure would obviously require etching the capacitor stack. There is a plate line electrode (cover Figure) and the hydrogen barrier is on the electrode and surrounds the capacitor.

13. With respect to claim 51, Bailey shows the use of a hydrogen barrier and Asano et al. show that oxygen can have deleterious effects and provides an oxygen barrier below the capacitor lower electrode (see cover Figure and column 17, line 30). It would be obvious to include an oxygen barrier in the Bailey device to prevent deleterious effects of oxygen as shown by Asano et al.

14. With respect to claim 52, Bailey does not describe the process of etching the capacitor stack but it is known in the art to provide a mask that does not etch to perform the etching and to do so would be obvious.

15. With respect to claims 53 and 54, Bailey describes the electrode thickness as 150 nm (column 8, line 28) but it would be obvious to use any thickness that had sufficiently low resistivity and since criticality has not been established it would be obvious to use these thicknesses.

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16. With respect to claim 55, Bailey does not describe the process of etching the capacitor stack but it is known in the art to provide a mask that does not etch to perform the etching and to do so would be obvious.

17. With respect to claim 56, Bailey does not specify that CMP is performed after other steps in the process but the use of CMP would be obvious in any case where the processed surface were insufficiently flat and would be performed for the same reason that the CMP shown is used.

18. Claims 57 and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bailey in view of Asano et al. and further in view of Kanaya et al.

19. With respect to claim 57, Bailey does not provide details of ferroelectric layer formation but Kanaya et al. shows (see Figures 4a, 4b and paragraphs 0084 and 0091) that the ferroelectric layer is crystallized and then patterned. It would be obvious to use this formation technique since it is known to be functional.

20. With respect to claim 58, annealing before or after patterning is a matter of design choice and it would be obvious to do either.

21. Claim 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bailey in view of Asano et al. and further in view of Fox et al.

22. Bailey does not provide details of ferroelectric layer formation but Fox et al. show that a PZT film of 180 nm (0040) is annealed at 600 degrees for 90 seconds. It would have been obvious to use this process since it is known to be functional and since criticality has not been established it would be obvious to form a thinner film as a matter of design choice.

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***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas A Wille whose telephone number is (571) 272-1721. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Douglas A. Wille  
Primary Examiner